

Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claim 1 (currently amended): An interconnect structure comprising:

a first planar network of electrical conductors formed in a first deposition process;

a second planar network of electrical conductors formed in a second deposition process, and separated from the first planar network by a separation region; and

a single interlevel dielectric material disposed within the separation region and extending into a portion of the first planar network, directly contacting and formed between successive metallization levels in an integrated circuit, without other intervening insulating materials between the first and second planar networks, successive metallization levels, the interlevel dielectric material comprising a polysiloxane network consisting essentially of silicon, oxygen, carbon and hydrogen and incorporating carbon-silicon bonding and having a dielectric constant of less than about 3.3.

Claim 2 (currently amended): The interlevel dielectric interconnect structure of Claim 1, having wherein the interlevel dielectric material has a dielectric constant of less than about 3.2.

Claim 3 (currently amended): The interlevel dielectric interconnect structure of Claim 1, having wherein the interlevel dielectric material has a carbon content of between about 5% and 20% relative to a silicon content.

Claim 4 (currently amended): The ~~interlevel dielectric interconnect structure~~ of Claim 1, wherein the ~~successive metallization levels~~ first and second planar networks comprise metal runners.

Claim 5 (currently amended): An integrated circuit ~~having an electrical path, the integrated circuit comprising:~~

a first ~~metallization level~~ planar network of electrical conductors formed in a first deposition process, and providing a first ~~portion of the~~ electrical path of the circuit;

a second ~~metallization level~~ planar network of electrical conductors formed in a second deposition process, and providing a second portion of the electrical path of the circuit, the second ~~metallization level~~ planar network separated from the first ~~metallization level~~ planar network by a gap; and

an interlevel dielectric material directly contacting the first and second ~~metallization levels~~ planar networks, and filling the gap between the first and second ~~metallization levels~~, planar networks, and extending into a portion of the first planar network, the interlevel dielectric material comprising polysiloxane, consisting essentially of silicon, oxygen, carbon and hydrogen and incorporating carbon therein and having a dielectric constant of less than about 3.5.

Claim 6 (currently amended): The integrated circuit of Claim 5, wherein the interlevel dielectric material has a dielectric constant of less than about 3.3.

Claim 7 (currently amended): The integrated circuit of Claim 6, wherein the first and second planar networks ~~comprise metallization levels~~ are metal runners.

Claim 8 (currently amended): The integrated circuit of Claim 6, wherein the first and second planar networks ~~comprise metallization levels~~ are transistor active areas within a semiconductor substrate.

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Claim 9 (currently amended): The integrated circuit of Claim 8, wherein the interlevel dielectric material comprises a sidewall spacer.

Claim 10 (cancelled).